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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/956,964	TANG, CHIH-CHIEN	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending and have been examined. The priority date considered for the application is September 21, 2001.

Claim Objections

2. Claim 1 objected to because of the following informalities: The terminology is not consistent, as the claim recites both an "update all" mode and a "to update all" mode, which likely refer to the same mode. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,275,931 to Narayanaswamy et al. (hereinafter "Narayanaswamy") in view of U.S. Pat. No. 5,603,055 to Evoy et al. (hereinafter "Evoy").

With respect to claim 1, Narayanaswamy discloses a method for updating a target computer by operating a remote computer connecting to the target computer and updating at least one of a boot block and a flash memory (see the abstract and FIG. 3, which shows a target computer 10 and a remote computer 32), comprising steps of:

(a) connecting serial port of the remote computer to serial port of the target computer with signal wires (see column 5, lines 16-22, which shows connecting the serial ports of the remote and target computers with a signal cable);

(b) providing modes of "not to update," "update the lock" and "update all" for user to select (see FIG. 4A, which shows an upgrade mode, i.e. a "not to update" mode, a boot code upgrade mode, i.e. an "update all" mode, and a main firmware upgrade mode, i.e. an "update the lock" mode);

(c) checking whether the mode is "not to update," and ending if the mode is (see FIG. 4A, which shows checking for the upgrade mode and ending the operation if instructed not to update);

(d) checking whether the mode is "update the lock" (see FIG. 4A, which shows checking for the main firmware upgrade mode);

(e) ending after updating flash memory of the target computer if the mode is "update the lock" (see FIG. 4A, which shows updating the main firmware and ending the operation, and column 4, lines 61-64, which further shows that the firmware is stored in flash memory);

(f) ending after updating boot block and flash memory of the target computer if the mode is "to update all" (see FIGS. 4A and 4B, which shows updating the boot code or boot block, updating the main firmware in flash memory, and ending the operation; note that "update all" is achieved by selecting to update the main firmware after the reset that follows an update to the boot code).

Although Narayanaswamy discloses updating the boot code and firmware of a device to enhance its functionality (see column 1, lines 20-30), Narayanaswamy does not

expressly disclose the limitation wherein firmware is a keyboard controller basic input/output system or BIOS.

However, Evoy discloses a keyboard controller BIOS (see keyboard controller 42 and BIOS ROM 20 in FIG. 2) for providing the necessary keyboard operating information to the computer system (see column 1, lines 20-44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of Narayanaswamy for updating a keyboard controller BIOS, such as the one taught by Evoy, in order to enhance the functionality of the keyboard controller.

5. Claims 2-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayanaswamy in view of Evoy as applied to claim 1 above, respectively, and further in view of U.S. Pat. No. 6,026,016 to Gafken (hereinafter "Gafken").

With respect to claim 2, although Narayanaswamy discloses providing modes (see FIG. 4A), Narayanaswamy does not expressly disclose the limitation wherein the step of providing modes is achieved by providing an updating control circuit and a lock control circuit for user to select.

However, in order to upgrade the boot code and firmware through the serial port (see column 5, lines 16-22), Narayanaswamy must inherently provide some form of updating control circuit. Furthermore, Gafken discloses a lock control circuit (see block locking circuit 140 in FIG. 1) for ensuring the integrity of data stored in flash memory, such as the BIOS and other boot code, and protecting the data from inadvertent overwriting (see column 1, lines 18-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the modes of Narayanaswamy by employing an updating control circuit, which is necessary to permit upgrading through the serial port, and a lock control circuit as taught by Gafken, to protect the firmware and boot code from unintended modifications when the other is updated.

With respect to claim 3, Narayanaswamy further discloses the limitation wherein the updating control circuit comprises a receiving controller for controlling signal receiving and a transmission controller for controlling signal transmission (see column 5, lines 16-22, which shows a standard serial interface; note that both a receiving controller and a transmission controller are inherent to the interface for enabling the communication of signals between the remote and target computers).

With respect to claim 4, Narayanaswamy does not expressly disclose the limitation wherein said receiving controller is a two for one multiplexer comprising:

(a) a first receiving input port connecting to SRXD of the target computer;

(b) a second receiving input port connecting to 8051RX of the target computer; and

(c) a receiving output port connecting to RXD of serial port of the target computer.

However, Evoy further discloses a multiplexer (see mux tree 40 in FIG. 2) that functions as a two-to-one multiplexer by arbitrating access to two separate sections of memory, the system BIOS and the keyboard controller BIOS (see column 4, lines 21-42). The keyboard controller is based on an 8051 microprocessor and therefore includes an

8051RX port for serial communications (see column 4, lines 42-53). Likewise, the serial interface of Narayanaswamy (see column 5, lines 16-22) inherently comprises the standard SRXD and RXD pins.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the receiving controller inherent to Narayanaswamy with a two-to-one multiplexer, as suggested by Evoy, to manage serial communications between the remote and target computers. The multiplexer circuit would realize the functionality disclosed by Narayanaswamy of providing a "not to update" mode and "update the lock" and "update all" modes (see FIG. 4A).

With respect to claim 5, Narayanaswamy does not expressly disclose the limitation wherein said transmission controller is a two for one multiplexer comprising:

(a) a first transmission input port connecting to STXD of the target computer;

(b) a second transmission input port connecting to 8051TX of the target computer; and

(c) a transmission output port connecting to TXD of serial port of the target computer.

However, Evoy further discloses a multiplexer (see mux tree 40 in FIG. 2) that functions as a two-to-one multiplexer by arbitrating access to two separate sections of memory, the system BIOS and the keyboard controller BIOS (see column 4, lines 21-42). The keyboard controller is based on an 8051 microprocessor and therefore includes an 8051TX port for serial communications (see column 4, lines 42-53). Likewise, the serial

interface of Narayanaswamy (see column 5, lines 16-22) inherently comprises the standard STXD and TXD pins.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the transmission controller inherent to Narayanaswamy with a two-to-one multiplexer, as suggested by Evoy, to manage serial communications between the remote and target computers. The multiplexer circuit would realize the functionality disclosed by Narayanaswamy of providing a "not to update" mode and "update the lock" and "update all" modes (see FIG. 4A).

With respect to claim 6, Narayanaswamy does not expressly disclose the limitations wherein:

(a) said first receiving input port is connected to said receiving output port, and said first transmission input port is connected to said transmission output port if the mode is "not to update;" and

(b) said second receiving input port is connected to said receiving output port, and said second transmission input port is connected to said transmission output port when the mode is one of "update the lock" and "update all."

However, Narayanaswamy discloses the "not to update" mode and the "update the lock" and "update all" modes (see FIG. 4A). Evoy further suggests a multiplexer for alternately enabling and disabling a connection to the keyboard controller BIOS (see column 4, lines 21-42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to control the upgrading disclosed by Narayanaswamy by connecting

ports of the serial interface and the keyboard controller according to the updating mode, in order to establish the appropriate connection for transmitting and receiving signals.

With respect to claim 7, Narayanaswamy does not expressly disclose the limitation wherein said lock controller is a two for one multiplexer comprising:

(a) a first lock input port connecting to power voltage of the target computer;

(b) a second lock input port connecting to ground; and

(c) a lock output port connecting to FWP# of the target computer.

However, Gafken further discloses that the lock controller (see block locking circuit 140 in FIG. 1) comprises an array of bits (see lock bit array 315 in FIG. 3), and that the bits are either set or cleared to control write access to the flash memory (see flash memory 115 in FIG. 1 and column 6, lines 19-36). The bits function as switches to connect either a voltage or a ground signal to the write protection logic of the flash memory, for ensuring the integrity of data stored therein, such as the BIOS and other boot code, and protecting the data from inadvertent overwriting (see column 1, lines 18-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the lock controller taught by Gafken as a switch or as an equivalent two-to-one multiplexer in order to protect the firmware and boot code of Narayanaswamy from unintended modifications when the other is updated.

With respect to claim 8, Narayanaswamy does not expressly disclose the limitations wherein:

(a) said first lock input port is connected to said lock output port when the mode is one of "not to update" and "update the lock;" and

(b) said second lock input port is connected to said lock output port when the mode is "update all."

However, Narayanaswamy discloses the "not to update" mode and the "update the lock" and "update all" modes (see FIG. 4A). Gafken further suggests a switch for alternately allowing or preventing writes to the flash memory (column 6, lines 19-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to control the upgrading disclosed by Narayanaswamy by connecting ports of the lock controller according to the updating mode, in order to permit or deny writes to the boot code and firmware as appropriate.

With respect to claim 9, the limitations recited in the claim are analogous to those of claims 1 and 2 (see the rationale applied to claims 1 and 2 above).

With respect to claim 10, the limitations recited in the claim are analogous to those of claim 3 (see the rationale applied to claim 3 above).

With respect to claim 11, the limitations recited in the claim are analogous to those of claim 4 (see the rationale applied to claim 4 above).

With respect to claim 12, the limitations recited in the claim are analogous to those of claim 5 (see the rationale applied to claim 5 above).

With respect to claim 13, the limitations recited in the claim are analogous to those of claim 6 (see the rationale applied to claim 6 above).

With respect to claim 14, the limitations recited in the claim are analogous to those of claim 7 (see the rationale applied to claim 7 above).

With respect to claim 15, the limitations recited in the claim are analogous to those of claim 8 (see the rationale applied to claim 8 above).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. U.S. Pat. No. 6,769,059 to Qureshi et al. discloses a system for updating a video BIOS without updating the entire system BIOS. U.S. Pat. No. 6,175,919 to Ha discloses a system for upgrading a BIOS using serial communication.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

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